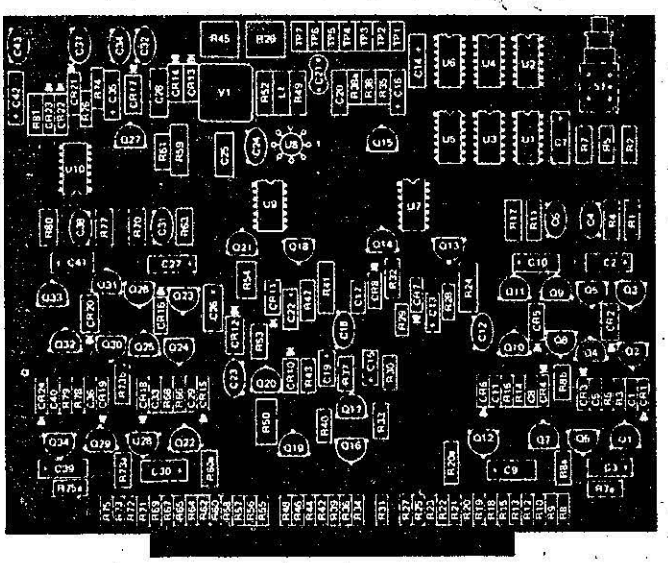
New Style.

NCR

M19-1 Terminal Clock Modules



Field Service and Training Manual

M19-1-STD TERMINAL CLOCK CONTENTS

CONTENTS

INTRODUCTION 1

GENERAL DESCRIPTION 2
Clock 2
Terminal Clock Initial Reset 2

LOGIC DESCRIPTION 2
Clock 3
Terminal Clock Initial Reset (TCIR) 3
Power-Up 3
Clock or Voltage Failure 4
Manual Control 4

SUMMARY 5

SERVICE INFORMATION 5

REVISION RECORD	
Date	Affected Pages/Remarks
Mar. 75	First Printing

ST-9152-19

M19-1-STD
TERMINAL CLOCK

INTRODUCTION

The M19-1-STD terminal clock module performs two functions for all units using an M115 or M15 terminal control unit (TCU) module as their base: generating clock, and monitoring logic voltages and clock. Clock pulses of the proper duration and frequency are generated for use by the MOS/LSI logic arrays in the modules of the parent unit. The +12 vdc and -12 vdc power supply outputs and the clock pulses generated by the terminal clock module are monitored by circuitry on the module.

The circuitry to perform the functions of the M19 terminal clock module consists of integrated circuits and discrete components. These components are mounted on an 8 inch by 10 inch printed circuit board. The connections between the terminal clock module and other modules within the parent unit are made through a 72-pin connector.

The M19-1-STD terminal clock module shown in the line drawing in Figure 1 is a replacement for the M19-1-STD (without change 7) and the M19-1-280. A line drawing and a schematic diagram covering both of the old style module assemblies are found on pages 6 and 7 .

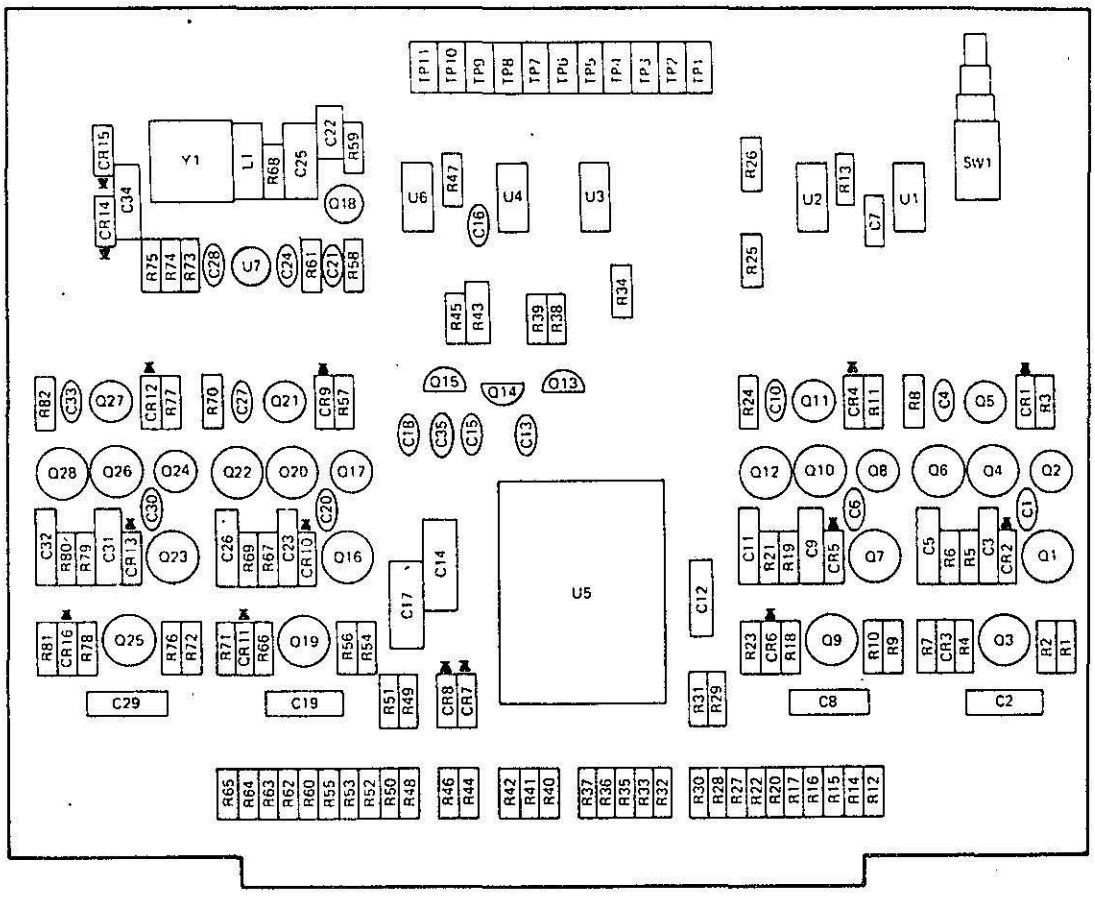


Figure 1 M19-1-STD terminal clock module

ST-9152-19

The general description and logic description which follow are applicable to the M19-1-STD (with change 7) as well as the two old style modules.

GENERAL DESCRIPTION

The clock module logic is divided into two sections: the clock generation section and the TCIR (Terminal Clock Initial Reset) section. The clock section generates two clock pulses (Phase 1 and Phase 3) needed to operate the MOS circuitry throughout the system (refer to Figure 2). The TCIR section supplies a reset signal to the system upon power up and also monitors power supply voltages and clock after power up. If clock or the voltages vary beyond specified tolerances, TCIR is generated and sent to the system. TCIR may also be manually controlled through the use of switch S1.

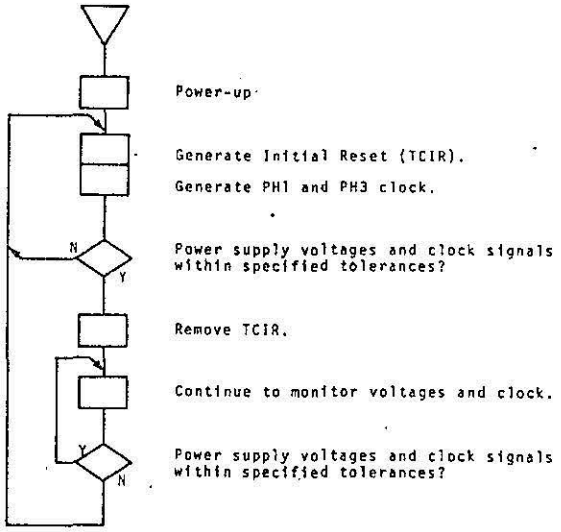


Figure 2 General operation flowchart

CLOCK

The Phase 1 and Phase 3 clock pulses are generated by dividing the output of the clock generator. The generator is an oscillator that begins operation during power-up. The output of the generator is applied to the clock divider. The divider has two outputs which control the PH1 and PH3 drivers. The drivers send the PH1 and PH3 clock signals to the system.

TERMINAL CLOCK INITIAL RESET

The terminal clock initial reset (TCIR) signal is generated anytime the monitored power supply voltages or clock signals vary from specified limitations. TCIR is always generated during power-up. Before TCIR can go High, the following conditions must be met.

1. Monitored power voltages must be within specified limitations.
2. The clock generator must be functioning properly.
3. Three DTCIR (Drop Terminal Control Initial Reset) pulses must be received from the system.
4. Three PH3 clock signals must be received from the clock divider coincident with the DTCIR pulses.
5. Manual control switch must be in the Off position.

TCIR is generated immediately during the operation of the system if any of the following conditions are detected.

1. Logic voltages vary outside specified limitations.
2. Clock generator frequency varies outside specified limtiations.
3. Manual control switch is moved to the On position.

LOGIC DESCRIPTION

The logical operations of the terminal clock module are presented in the following descriptions. Gate-by-gate circuit descriptions are not provided. Monitoring circuits, driver circuits, and the clock generator are illustrated in block form (Figure 3) with reference made only to voltages and terms which are significant to the logic operation. The module schematic shown on pages 8 and 9 is divided into the same logical blocks as shown in the block diagram.

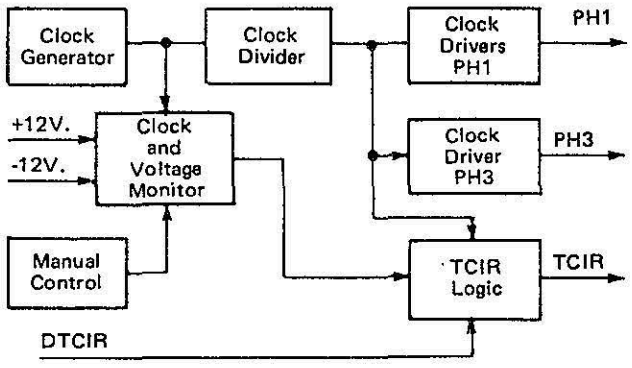


Figure 3 Module block diagram

M19-1-STD TERMINAL CLOCK

CLOCK

The PH1 and PH3 clock logic shown in Figure 4 consists of the following sections.

1. Clock generator
2. Divide-by-six counter
3. Two NAND gates
4. Two clock drivers

The clock signals from the generator are input to the divide-by-six counter. The outputs from the counter are applied to the two NAND gates. The gates decode the phase (either one or three) and select the proper driver.

The clock generator is a crystal controlled oscillator which operates at 864kHz. The generator begins operating as soon as power is up. The pulses from the generator are applied to the clock inputs of the three flip-flops in the divide-by-six counter. The counter advances with the fall of each clock pulse. The 864kHz signal is also supplied to the system through gate N3 which feeds pin 25 of the 72-pin connector.

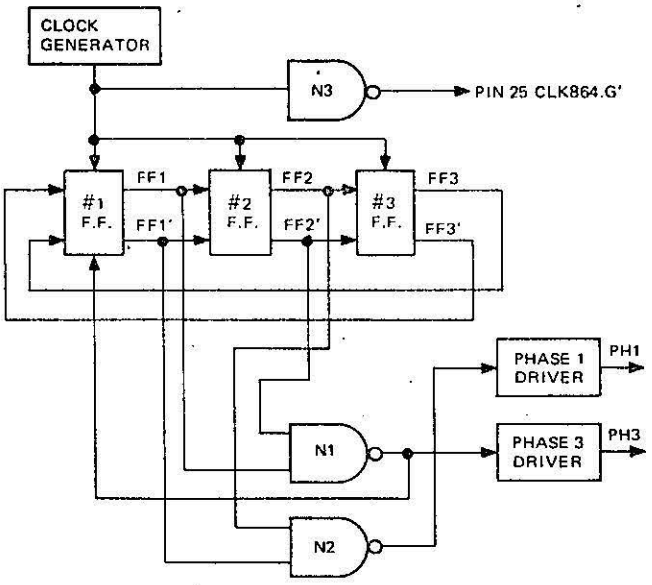


Figure 4 Clock logic

The divide-by-six counter is a three-position Johnson counter. The outputs of the counter are decoded by gates N1 and N2. N1 decodes PH3 clock and N2 decodes PH1 clock. The outputs of the decode gates are applied to their respective clock drivers. Figure 5 illustrates the timing used to divide and decode the 864kHz clock.

Figure 6 shows the clock lines leaving the drivers and the connector pins to which the lines are connected. The clock lines are any lines with

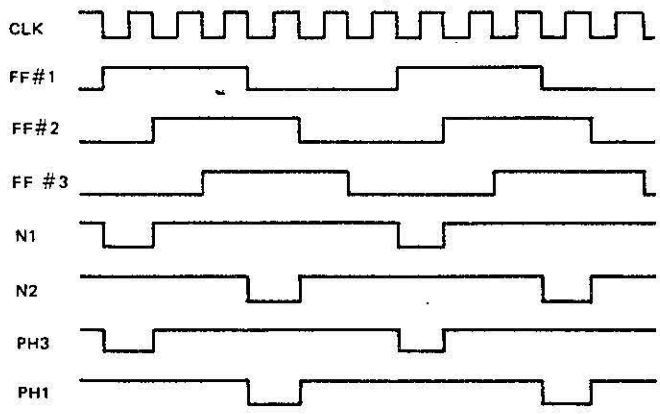


Figure 5 Clock timing

the mnemonics containing the letter J, such as PH1.JBA. The remainder of the lines are shields for the clock lines (e.g., PH1.QBA).

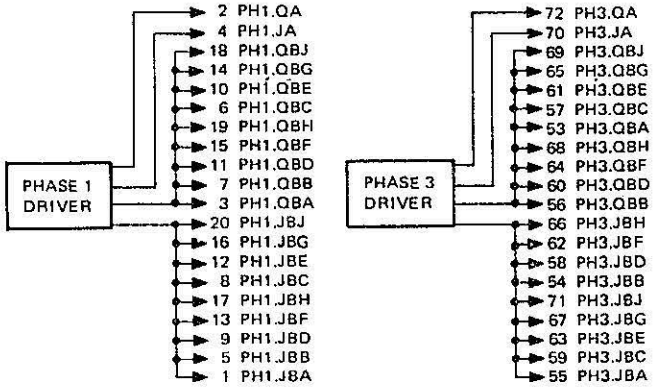


Figure 6 Clock drivers

TERMINAL CLOCK INITIAL RESET (TCIR)

The TCIR logic consists of the following groups of circuitry.

1. Clock and voltage monitor
2. Manual control logic
3. Five nand gates
4. Three-position counter
5. TCIR driver/bipolar-to-MOS converter

TCIR is controlled by a three-position counter (Figure 7). Whenever the counter is not at a count of three, the TCIR line is taken Low to reset the logic in all modules in the system. The counter is not at a count of three during power up, when a clock or voltage supply failure is detected, or manual control is exercised.

POWER-UP

The counter consisting of flip-flops 4, 5, and 6 is

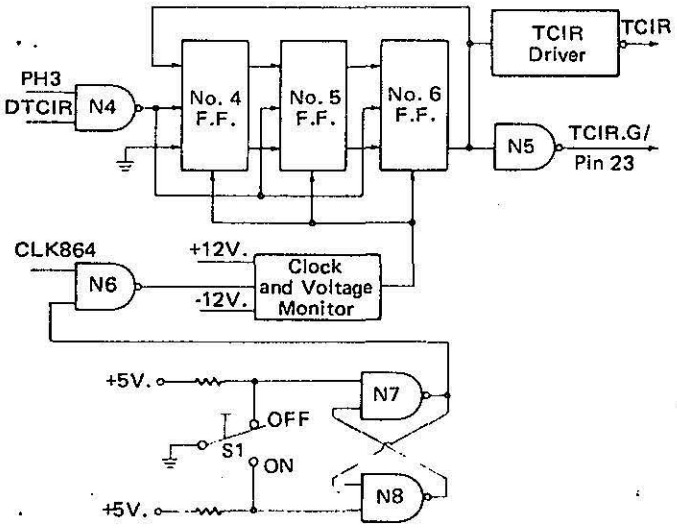


Figure 7 TCIR logic

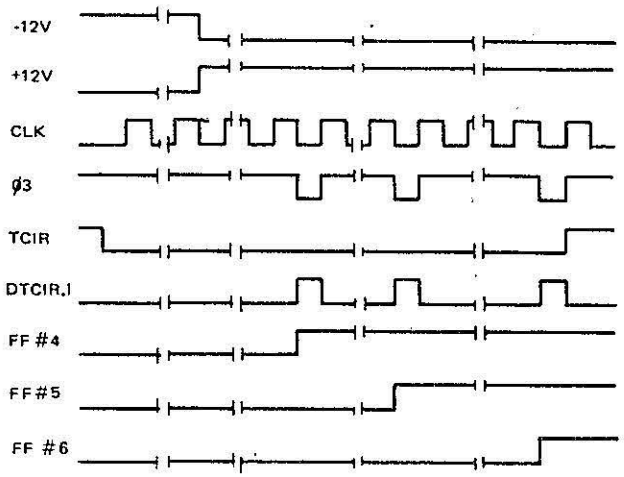


Figure 8 TCIR timing

reset during power-up by the clock and voltage monitor reset signal. The reset signal is activated when the monitor determines that the proper operating levels have not been attained.

When the flip-flops are reset, a High signal from flip-flop 6 is applied to the TCIR driver/bipolar-to-MOS converter. The driver/converter which is necessary to make the TTL logic of the terminal clock module compatible with the MOS logic of the system sends the initial reset to the modules in the system. A TTL initial reset signal (TCIR.G/) is also sent to the system through pin 23 of the 72-pin connector for use by modules containing TTL logic (e.g., M17 read/write memory).

TCIR remains low until the three-position counter attains the count of three. The counter cannot begin counting until a DTCIR pulse is received coincident with the PH3 signal from the clock section. A DTCIR pulse is generated in the TCU every TP16 time. There is an interval of 111 microseconds between TP16 times (one TCU character time).

The three-position counter is advanced by one each time the counter clock input goes Low. The signal to the counter clock inputs is made through gate N4 which is controlled by DTCIR.I from the TCU module and PH3 clock from the clock input signal to advance the counter. After receiving the third clock input signal, the counter holds and disregards further clock pulses. TCIR is disabled until the counter flip-flops are again reset.

The TCIR timing sequence during power-up is illustrated in Figure 8.

CLOCK OR VOLTAGE FAILURE

TCIR may also be generated anytime during the operation of the system if the clock and voltage monitor circitry senses a failure of the clock or logic voltages. When a failure is sensed, the reset output of the monitor circuitry goes Low resetting the flip-flops in the three-position TCIR counter. The initial reset signal (TCIR) is generated as a result of resetting the counter flip-flops. Before TCIR can be disabled, the reset signal must be removed from the counter. If the failure causing the reset is due to voltage fluctuation or noise, the monitor detecting the failure switches its output back to normal as soon as the disturbance has subsided. If the reset is due to a consistent failure of the monitored circuit, the circuit at fault must be repaired before normal operation may resume.

Removal of TCIR from the system beings when the monitor removes the reset from the three-position counter and the first DTCIR.I is received from the TCU. The three-position counter then advances by one with each DTCIR.I pulse and PH3 clock. When the counter reaches the count of three, flip-flop 6 disables the TCIR driver/bipolar-to-MOS converter removing TCIR from the system.

MANUAL CONTROL

TCIR may also be generated by pressing the manual control switch (S1) to the On position. Pressing S1 sets the latch consisting of N7 and N8. The output of N7 switches Low when the switch is pressed. This Low output is input to N6 to simulate a loss of clock. The voltage and clock monitor circuitry senses the apparent loss of clock and, as a result, causes the reset output to go Low to reset the three-position TCIR counter. Resetting

M19-1-STD TERMINAL CLOCK

the counter flip-flops causes initial reset (TCIR) to be generated.

The counter remains reset until S1 is restored to the Off position. When S1 is restored, the latch switches state allowing the clock signal to be input to the monitor circuitry. Sensing the restoration of clock, the monitor removes the reset input to the TCIR counter. After three DTCIR.I pulses and PH3 clocks are received, the counter removes TCIR from the system.

Figure 9 shows the TCIR lines leaving the TCIR driver and the connector pins to which the lines are connected. The TCIR lines are the lines with the mnemonic containing the letter J. The remainder of the lines are shields for the TCIR lines.

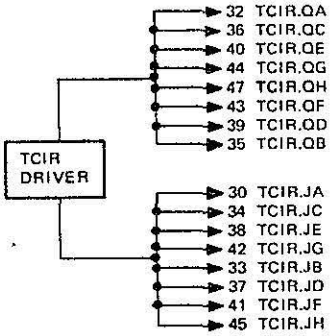


Figure 9 TCIR driver

A summary of TCIR operation is shown in the flow chart in Figure 10.

SUMMARY

The M19-1-STD terminal clock module generates phase 1 (PH1) and phase 3 (PH3) clock signals for use by all MOS/LSI logic within the unit. The module circuitry also ensures proper unit logic operation by supplying an initial reset signal (TCIR) to the parent unit modules during power up-sequence, when a power supply voltage drops below specified limits, or when either phase clock is lost.

SERVICE INFORMATION

The M19-1-STD terminal clock module is provided with test points to aid the NCR Field Engineer in isolating system malfunctions caused by the M19-1-STD to the module. The table in Figure 11 shows the seven test points and the signal that can be monitored at each test point.

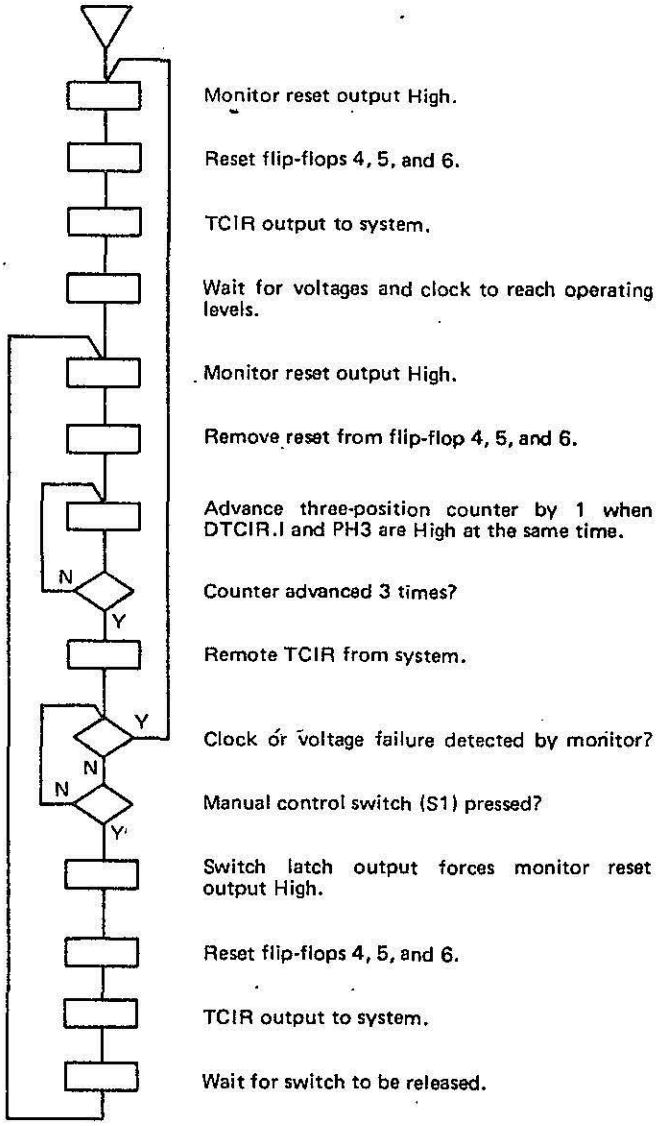
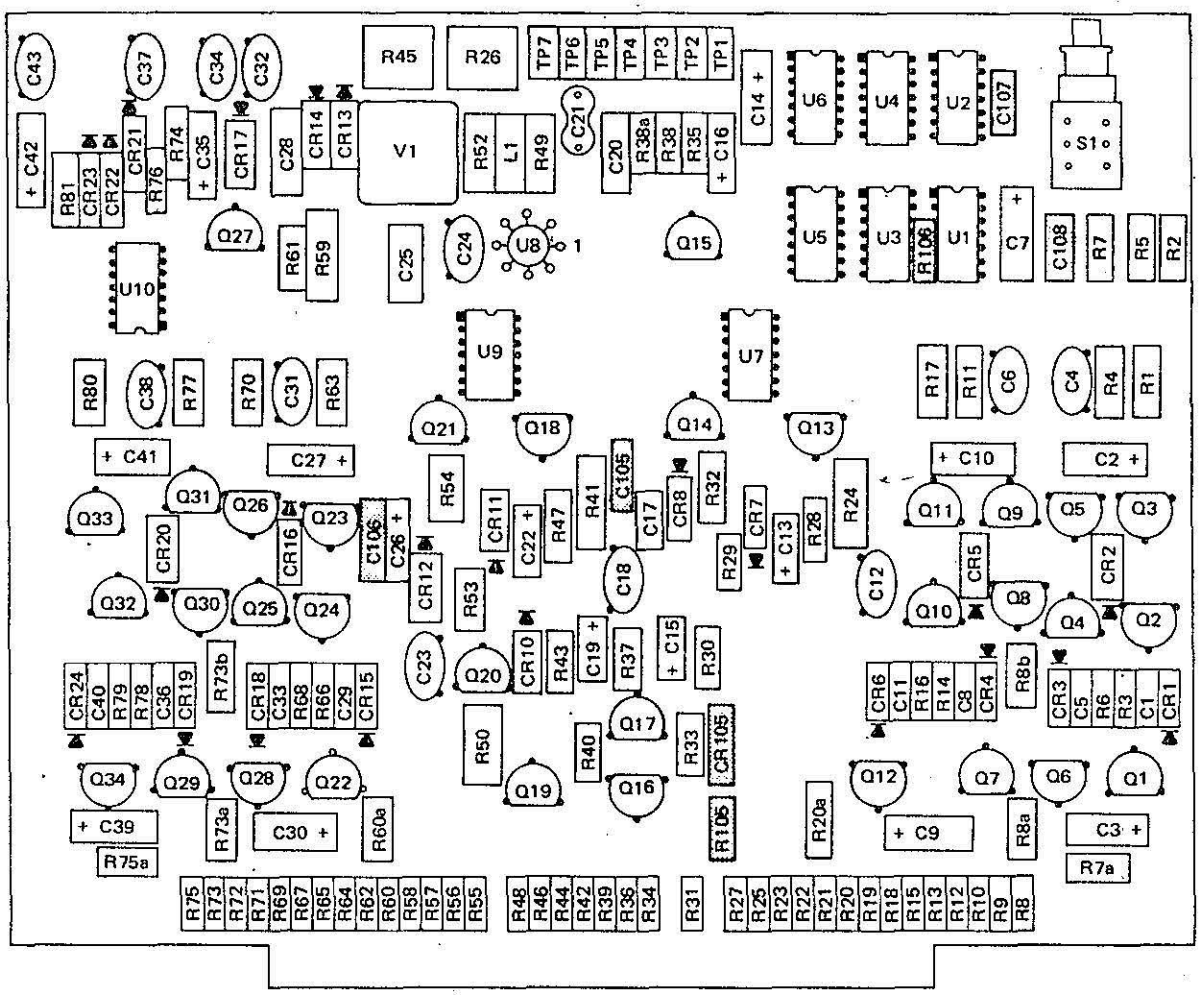

Monitor reset output High.
Reset flip-flops 4, 5, and 6.
TCIR output to system.
Wait for voltages and clock to reach operating levels.
Monitor reset output High.
Remove reset from flip-flop 4, 5, and 6.
Advance three-position counter by 1 when DTCIR.I and PH3 are High at the same time.
N
Counter advanced 3 times?
Y
Remote TCIR from system.
Y
Clock or voltage failure detected by monitor?
N
N
Manual control switch (S1) pressed?
Y
Switch latch output forces monitor reset output High.
Reset flip-flops 4, 5, and 6.
TCIR output to system.
Wait for switch to be released.

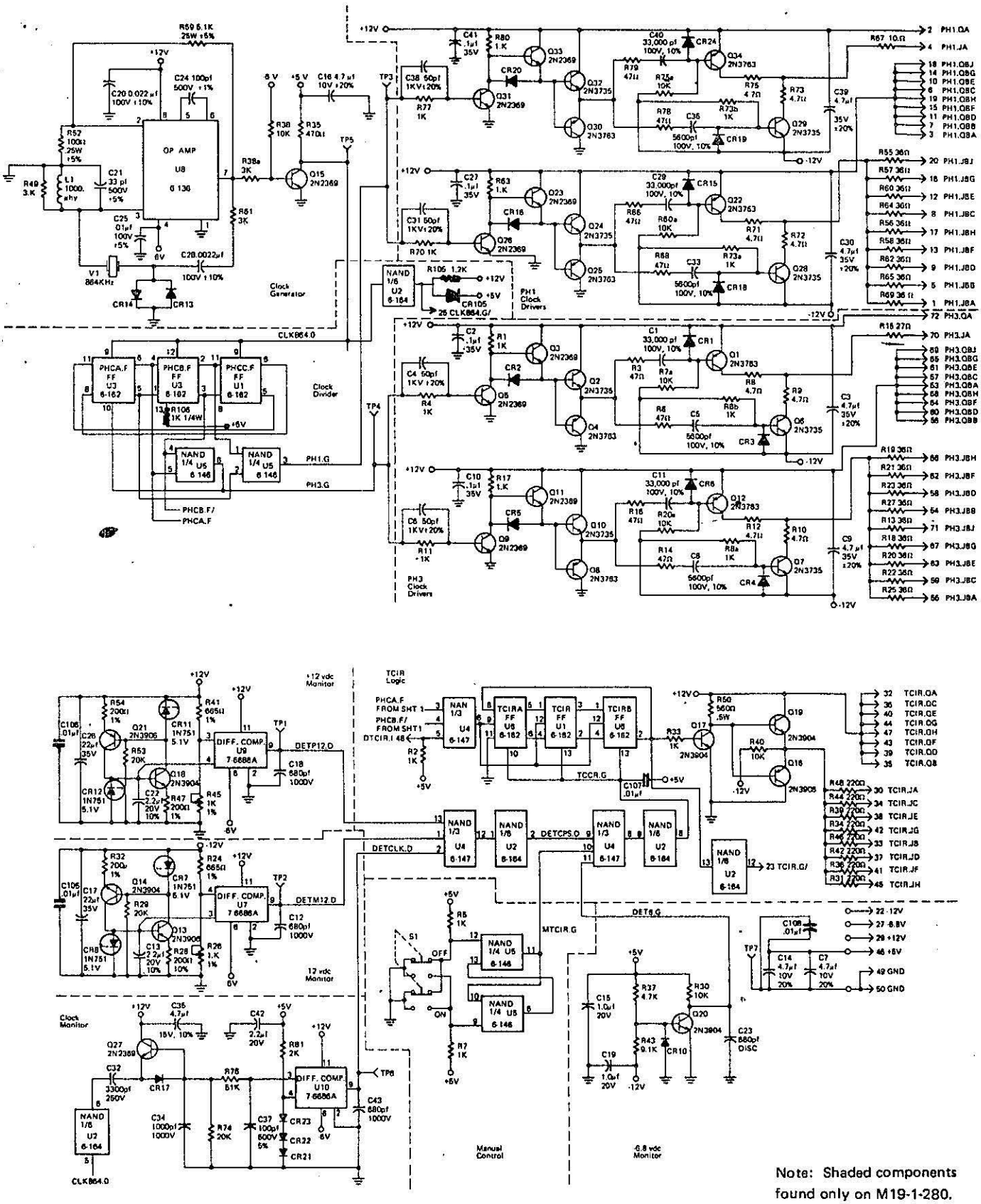
Figure 10 TCIR operation flow chart

Test Point	Function
TP1	+12 vdc monitor; this test point is at logic ONE when +12 vdc power supply output is at least +11.04 vdc.
TP2	-12 vdc monitor; this test point is at logic ONE when -12 vdc power supply output is at least -11.04 vdc.
TP3	Phase 1 clock; signal at the test point goes from +5 vdc to 0 vdc for 1.157 μsec. every 6.94 μsec.
TP4	Phase 3 clock; signal at this test point goes from +5 vdc to 0 vdc for 1.157 μsec. every 6.94 μsec. Ph3 is approximately 3.5 μsec. after PH1.
TP5	864kHz clock; signal at this test point is a square wave having a 1.157 μsec. cycle time. The signal varies between +5 vdc and 0 vdc.
TP6	Clock monitor; this test point is at logic ONE when the 864kHz clock generator circuit is operable.
TP7	Logic ground.

Figure 11 M19-1-STD test points table

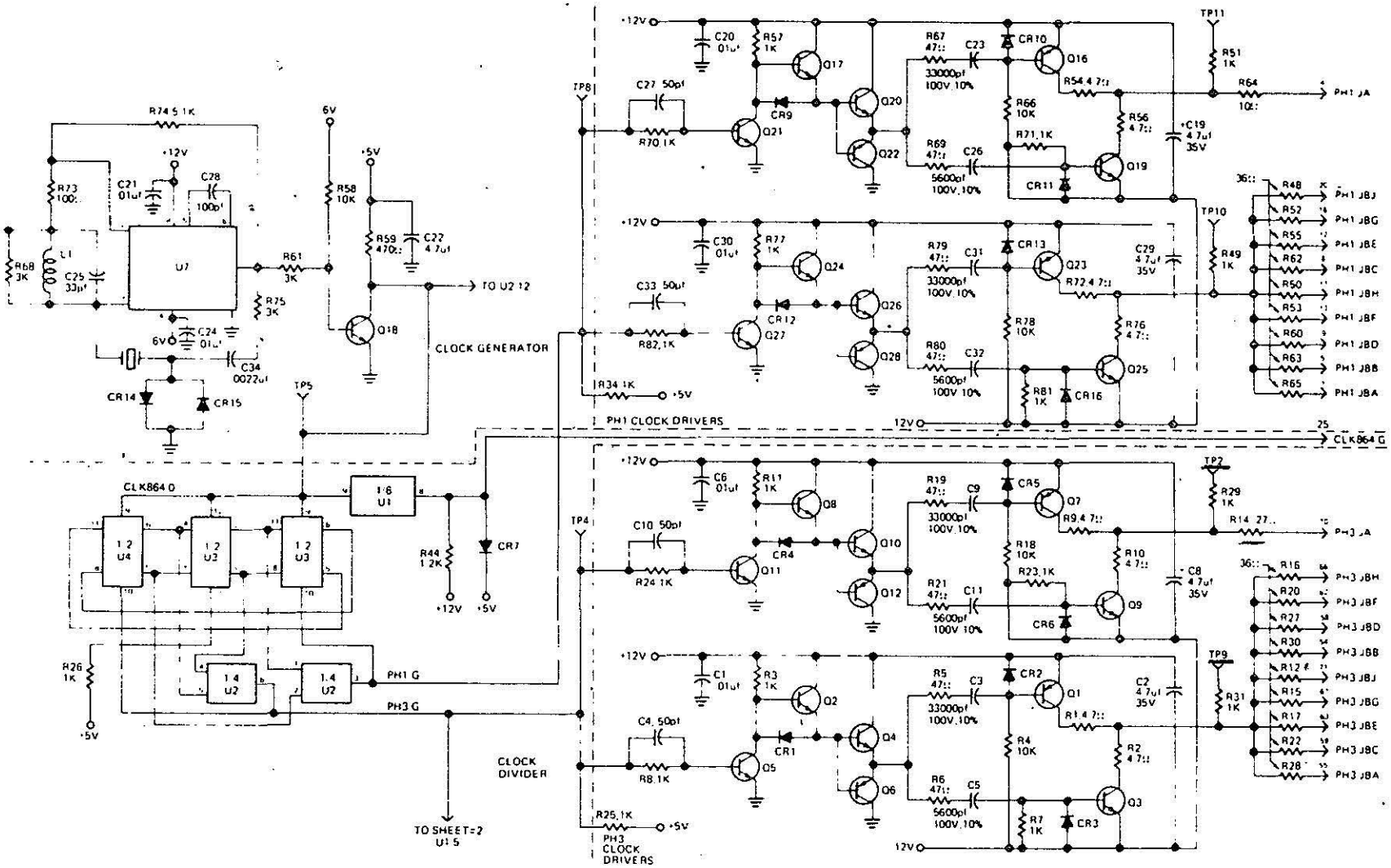


M19-1-STD,(without chg 7; shaded components excluded)
M19-1-280 (shaded components included)



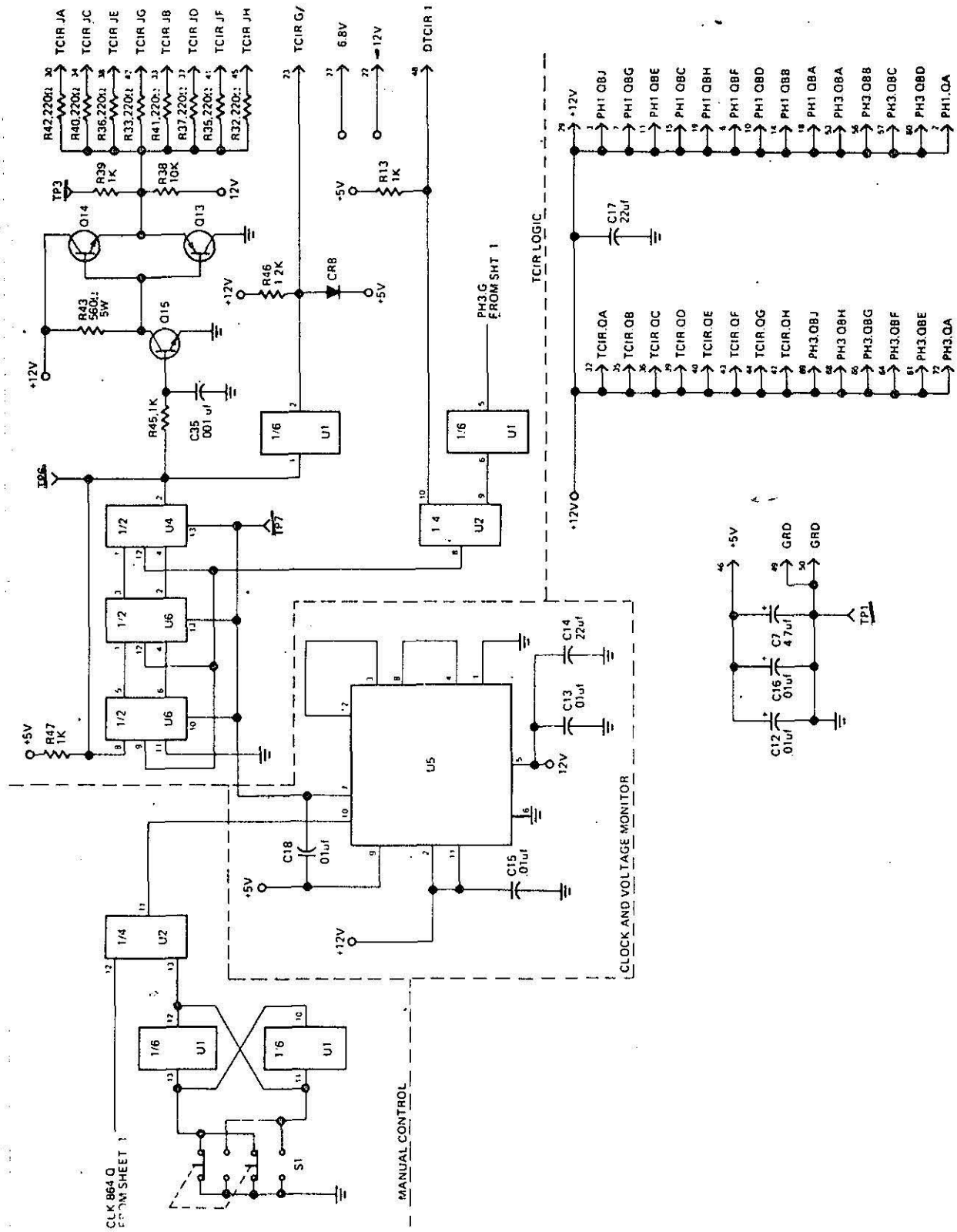
Note: Shaded components found only on M19-1-280.

) M19-1-STD (w/o chg 7)/M19-1-280 schematic



M19-1-STD (w/chg 7) schematic (1 of 2)

M19-1-STD TERMINAL CLOCK

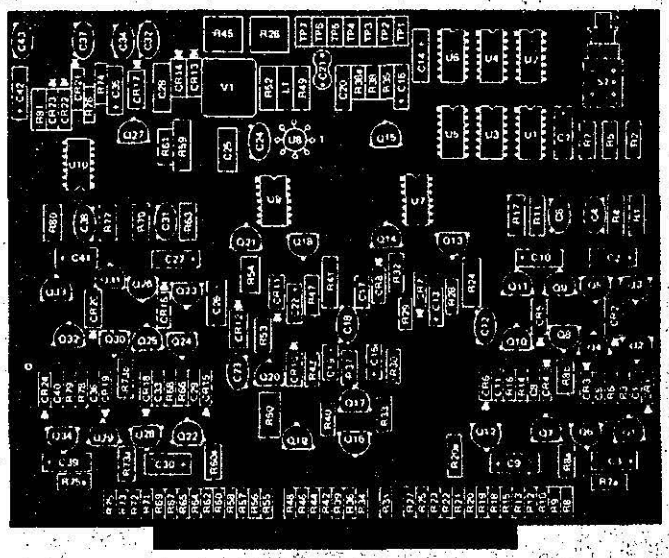


M19-1-STD (w/chg 7) schematic (2 of 2)

Old Style.

NCR

M19-1 Terminal Clock Modules



Field Service and Training Manual

Prepared By
Technical Publications Department
Corporate Education Division

M19-1
TERMINAL CLOCK MODULES

FIELD SERVICE
AND TRAINING MANUAL

MS-419
Rev. 1
Jan. 15, 1974

This is a revision of a manual previously titled

M-19-1-STD
TERMINAL CLOCK MODULE
FIELD SERVICE AND TRAINING MANUAL

Copyright © 1972, 1974
The National Cash Register Company
Dayton, Ohio, United States of America
All Rights Reserved
Printed in U.S.A.

REVISION RECORD

M19-1 TERMINAL CLOCK MODULES

FIELD SERVICE AND TRAINING MANUAL

REV. NO.	DATE	AFFECTED PAGES/REMARKS
	7-15-72	First Printing
1	1-15-74	Added: References to M19-1-280 in text and illustrations

This manual is written to the following change levels

MODULE	CHG LEVEL
M19-1-STD	5
M19-1-280	1

M19-1
TERMINAL CLOCK MODULES
FIELD SERVICE AND TRAINING MANUAL

SCOPE

The purpose of this manual is to describe the physical characteristics, the functions, and the general operation of the M19-1 terminal clock modules. The description is in sufficient detail to permit isolation of system malfunctions caused by the terminal clock modules.

As a prerequisite to using this manual, the reader should be familiar with the information contained in *Basic Terminal Concepts* (MS-841).

CONTENTS

INTRODUCTION 1
GENERAL DESCRIPTION 1
Clock 1
Terminal Clock Initial Reset 2
LOGIC DESCRIPTION 2
Clock 2
Terminal Clock Initial Reset 3
Power-Up 3
Clock or Voltage Failure 4
Manual Control 4
SUMMARY 5
SERVICE INFORMATION 5
SCHEMATIC . . . . . App. 1

M19-1
TERMINAL CLOCK MODULES

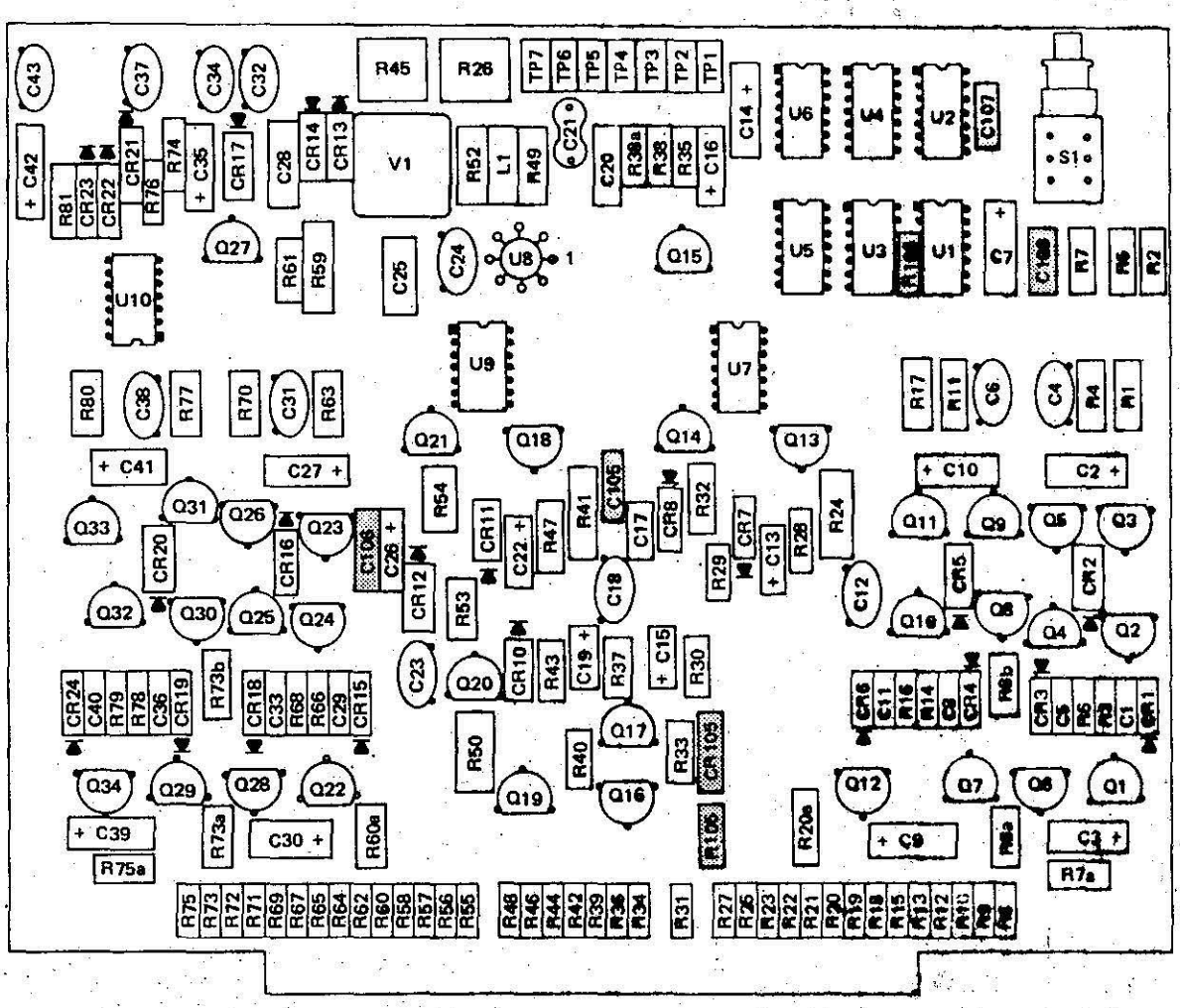


Fig. 1 M19-1 terminal clock module

INTRODUCTION

The M19-1 terminal clock modules perform two functions for all units using an M15 terminal control unit (TCU) module as a base: generating clock and monitoring logic voltages and clock. Clock pulses of the proper duration and frequency are generated for use by the MOS/LSI logic arrays in the modules of the parent unit. The +12 v.d.c., -12 v.d.c., and -6.8 v.d.c. power supply outputs and the clock pulses generated by the M19-1 are monitored by circuitry on the terminal clock module.

The circuitry to perform the functions of the module consists of integrated circuits and discrete components. These components are mounted on an 8 inch by 10 inch printed circuit board. The connections between the terminal clock module and other modules in the parent unit are made through a 72-pin connector.

Currently there are two M19-1 terminal clock modules in use: the M19-1-STD and the M19-1-280. The two modules are functionally identical and are electrically and physically interchangeable. The M19-1-280 is less susceptible to electrical noise than the M19-1-STD.

A line drawing of an M19-1 is shown in figure 1. The components highlighted with shading are found only on the M19-1-280.

GENERAL DESCRIPTION

The clock module logic is divided into two sections: the clock generation section and the TCIR (Terminal Clock Initial Reset) section. The clock section generates two clock pulses (phase 1 and phase 3) needed to operate the MOS circuitry throughout the system (refer to fig. 2). The TCIR section supplies a reset signal to the system upon power up and also monitors three power supply voltages and clock after power up. If clock or any of the voltages vary beyond specified tolerances, TCIR is generated and sent to the system. TCIR may also be manually controlled.

A switch located on the upper right-hand corner of the clock card provides manual control of TCIR.

CLOCK

The phase 1 and phase 3 clock pulses are generated by

dividing the output of the clock generator. The generator is an oscillator that begins operation during power-up. The output of the generator is applied to the clock divider. The divider has two outputs which control the PH1 and PH3 drivers. The drivers send the PH1 and PH3 clock signals to the system.

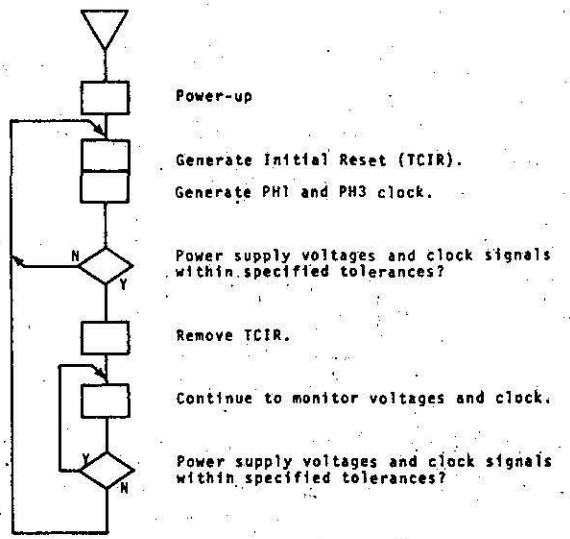


Fig. 2 General operation flow chart

TERMINAL CLOCK INITIAL RESET

The terminal clock initial reset (TCIR) signal is generated anytime the monitored power voltages or clock signals vary from specified limitations. TCIR is always generated during power-up. Before TCIR can go High, the following conditions must be met.

1. Monitored power voltages must be within specified limitations.
2. The clock generator must be functioning properly.
3. Three DTCIR (Drop Terminal Control Initial Reset) pulses must be received from the system.
4. Three PH3 clock signals must be received from the clock divider coincident with the DTCIR pulses.
5. Manual control switch must be in the OFF position.

TCIR is generated immediately during the operation of the system if any of the following conditions are detected.

1. Logic voltages vary outside specified limitations.
2. Clock generator frequency varies outside specified limitation.
3. Manual control switch is moved to the ON position.

LOGIC DESCRIPTION

The logical operations of the terminal clock module are presented in the following descriptions. Gate-by-gate circuit descriptions are not provided. Monitoring circuits, driver circuits, and the clock generator are illustrated in block form (figure 3) with reference made only to voltages and terms which are significant to the logic operation. The module schematic shown in the appendix is divided into the same logical blocks as shown in the block diagram.

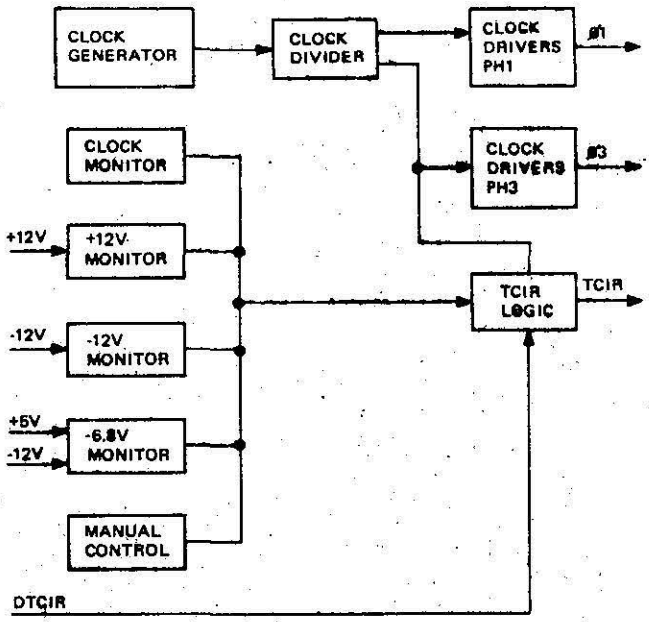


Fig. 3 M19-1 block diagram

CLOCK

The PH1 and PH3 clock logic shown in figure 4 consists of the following sections.

1. Clock generator
2. Divide-by-six counter
3. Two NAND gates
4. Two clock drivers

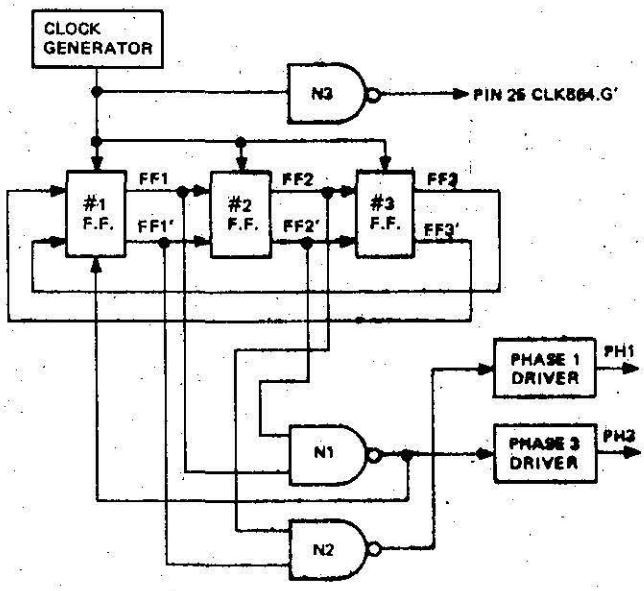


Fig. 4 Clock logic

The clock signals from the generator are input to the divide-by-six counter. The outputs from the counter are applied to the two NAND gates. The gates decode the phase (either one or three) and select the proper driver.

The clock generator is a crystal controlled oscillator which operates at 864 kHz. The generator begins operating as soon as power is up. The pulses from the generator are applied to the clock inputs of three flip-flops in the divide-by-six counter. The counter advances with the fall of each clock pulse. The 864 kHz signal is also supplied to the system through gate N3 which feeds pin 25 of the 72-pin connector.

The divide-by-six counter is a three-position Johnson counter. The outputs of the counter are decoded by gates N1 and N2. N1 decodes PH3 clock and N2 decodes PH1 clock. The outputs of the decode gates are applied to their respective clock drivers. Figure 5 illustrates the timing used to divide and decode the 864 kHz clock.

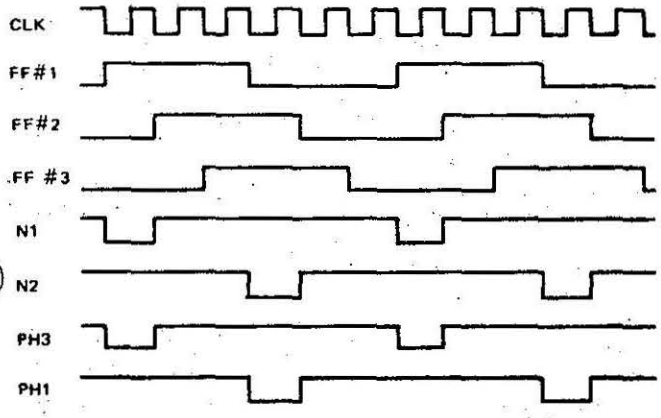


Fig. 5 Clock timing

Figure 6 shows the clock lines leaving the drivers and the connector pins to which the lines are connected. The clock lines are any lines with the mnemonics containing the letter J, such as PH1.JBA. The remainder of the lines are shields for the clock lines.

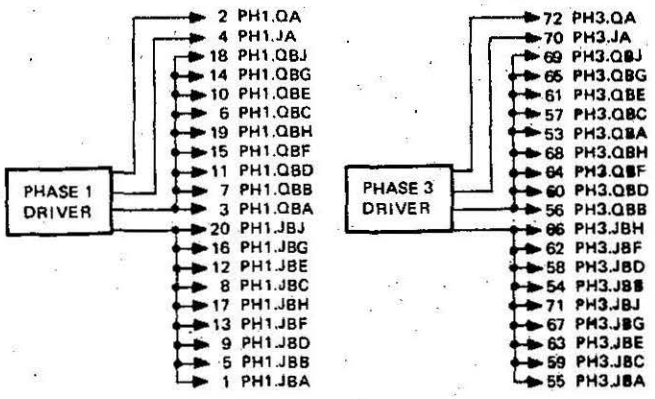


Fig. 6 Clock drivers

TERMINAL CLOCK INITIAL RESET (TCIR)

The TCIR logic consists of the following groups of circuitry.

1. +12 v. monitor
2. -12 v. monitor
3. -6.8 v. monitor
4. Clock monitor
5. Manual control logic
6. Five nand gates
7. Three-position counter
8. TCIR driver/bipolar to MOS converter.

TCIR is controlled by a three-position counter (refer to fig. 7). Whenever the counter is not at a count of three, the TCIR line is taken Low to reset the logic in all modules in the system. The counter is not at a count of three during power up, when a clock or voltage supply failure is detected, or manual control is exercised.

POWER-UP

The counter is reset during power-up. During power-up, the clock monitor and voltage monitors detect that proper operating levels have not been attained. The monitors send a reset signal through gates N4 and N5 to the three-position counter. The three-position counter consists of F.F. No. 4, F.F. No. 5, and F.F. No. 6. The flip-flops reset and the No. 6 F.F. applies a High signal to the TCIR driver/bipolar to MOS converter. The driver/converter sends TCIR to the system. The converter is necessary to make the TTL logic used on the clock card compatible with the system MOS logic. A direct TCIR is also sent to the system through N8 which feeds pin 23 of the 72-pin connector.

TCIR remains Low until the three-position counter attains the count of three. The counter cannot begin counting until a DTCIR pulse is received coincident with a PH3 being decoded in the clock section. A DTCIR pulse is generated in the TCU every TP16 time. There is an interval of 111 microseconds between TP16's (one character time).

The three-position counter is advanced by one each time the counter clock input goes Low. The counter clock inputs are controlled by gate N8. Gate N8 is controlled by DTCIR.I, F.F.1, and F.F.2. The F.F.1 and F.F.2' signals are received from the divide-by-six counter in the clock circuit. Both F.F.1 and F.F.2' are High when PH3 clock is being decoded. DTCIR.I is received from the TCU every 111 microseconds. Every 111 microseconds all three signals (F.F.1, F.F.2', and DTCIR.I) are High at gate N8, and a clock pulse is sent to the three-position counter advancing it by one. Upon reaching the count of three, the counter holds and disregards further clock pulses. TCIR is disabled until the three-position counter is reset.

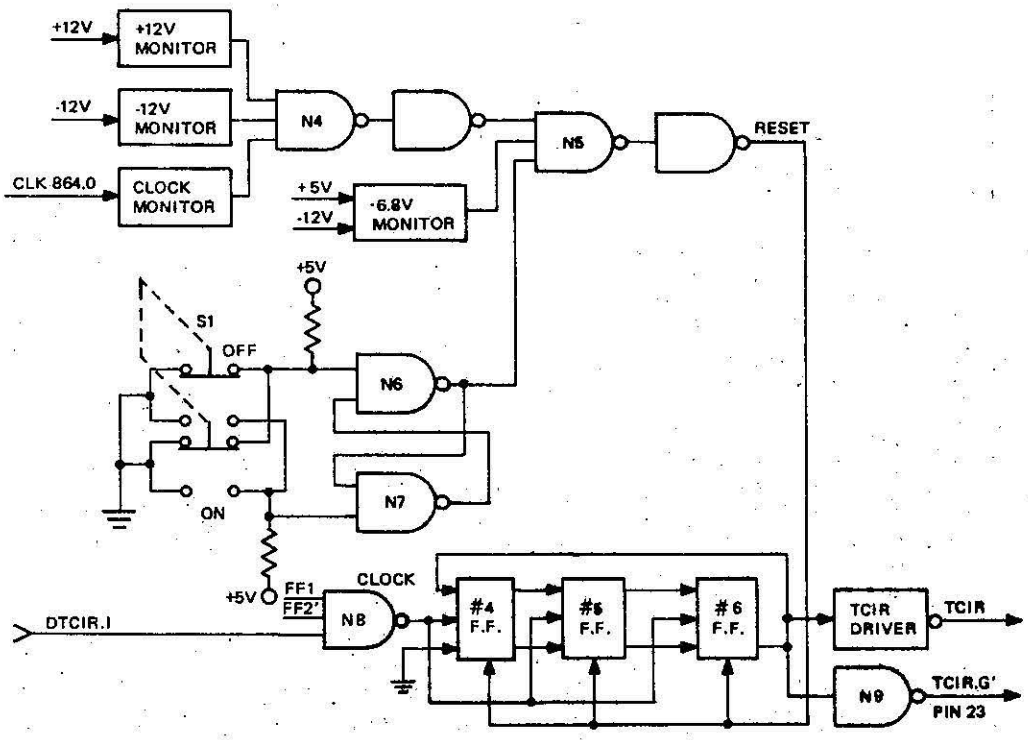


Fig. 7 TCIR logic

The TCIR sequence during power-up is illustrated in figure 8.

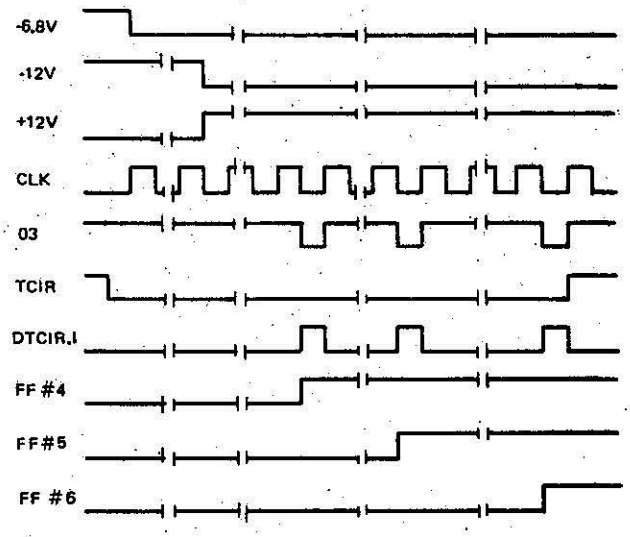


Fig. 8 TCIR timing

CLOCK OR VOLTAGE FAILURE

TCIR is also generated anytime during the operation of the system if the clock monitor or any of the voltage monitors detect a failure. The monitor detecting the failure forces gate N5 to switch its output. The output of N5 goes High, is inverted Low, and applied to the direct reset positions of the three-position counter. The counter resets, and the output of F.F.No.6 brings TCIR Low. Before TCIR can be disabled, the reset signal must be removed from the counter. If the failure causing the reset is due to voltage fluctuation or noise, the monitor detecting the failure switches its output back to normal as soon as the disturbance has subsided. If the reset is due to a consistent failure of the monitored circuit, the circuit at fault must be repaired before normal operation may resume.

Removal of TCIR from the system begins when the monitor detecting the failure removes the reset from the three-position counter and the first DTCIR.I is received from the TCU. The three-position counter then advances by one with each DTCIR.I pulse and PH3 clock. When the counter reaches the count of three,F.F.No. 6 disables the TCIR driver/bipolar-to-MOS converter and TCIR is removed from the system.

MANUAL CONTROL

TCIR is also generated by moving the manual control switch S1 to the ON position. S1 controls a latching circuit which consists of N6 and N7. With the switch in the OFF position, the output of the latch is High. By moving S1 to ON, the latch switches state and the output of the latch goes Low. The output of the latch (gate N6) switches the output of gate N5, generating a reset pulse to the three-position counter. The counter resets and ables the TCIR driver/bipolar-to-MOS converter.

The counter remains reset until S1 is restored to the OFF position. When S1 is restored, the latch switches state and removes the disabling signal from N5. Gate N5 removes the reset from the three-position counter. Upon receipt of three DTCIR.I pulses and PH3 clocks, the three-position counter removes TCIR from the system.

Figure 9 shows the TCIR lines leaving the TCIR driver and the connector pins to which the lines are connected. The TCIR lines are the lines with the mnemonic containing the letter J. The remainder of the lines are shields for the TCIR lines.

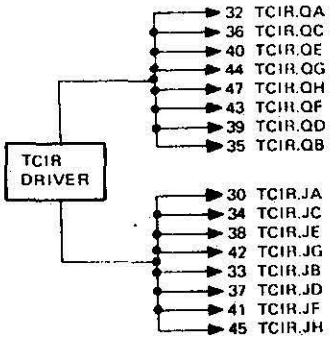


Fig. 9 TCIR driver

A summary of TCIR operation is shown in the flow chart in figure 10.

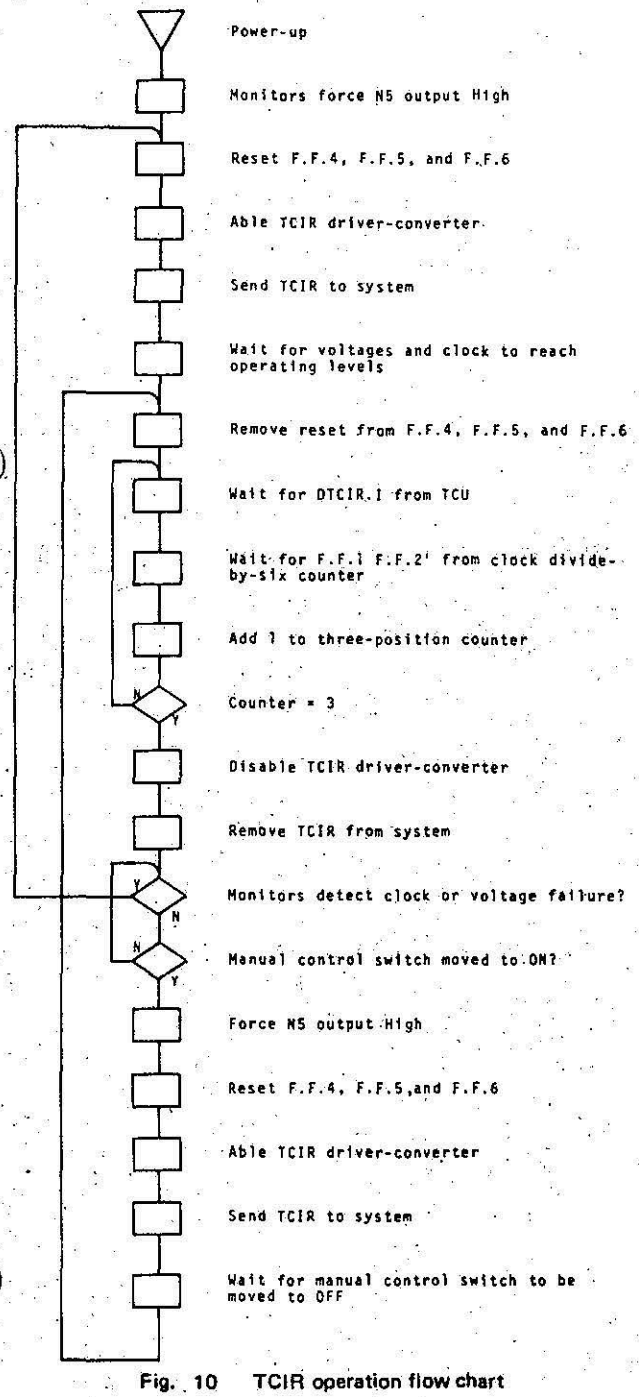

Power-up
Monitors force N5 output High
Reset F.F.4, F.F.5, and F.F.6
Able TCIR driver-converter
Send TCIR to system
Wait for voltages and clock to reach operating levels
Remove reset from F.F.4, F.F.5, and F.F.6
Wait for DTCIR.I from TCU
Wait for F.F.1 F.F.2' from clock divide-by-six counter
Add 1 to three-position counter
Counter = 3
N
Y
Disable TCIR driver-converter
Remove TCIR from system
Monitors detect clock or voltage failure?
Y
N
Manual control switch moved to ON?
N
Y
Force N5 output High
Reset F.F.4, F.F.5,and F.F.6
Able TCIR driver-converter
Send TCIR to system
Wait for manual control switch to be moved to OFF

Fig. 10 TCIR operation flow chart

SUMMARY

The M19-1 terminal clock modules generate phase 1 (PH1) and phase 3 (PH3) clock signals for use by all MOS/LSI logic arrays within the unit. The circuitry also ensures proper unit logic operation by supplying an initial reset signal (TCIR) to the parent unit modules during power up-sequence, when a power supply voltage drops below specified limits, or when either phase clock is lost.

SERVICE INFORMATION

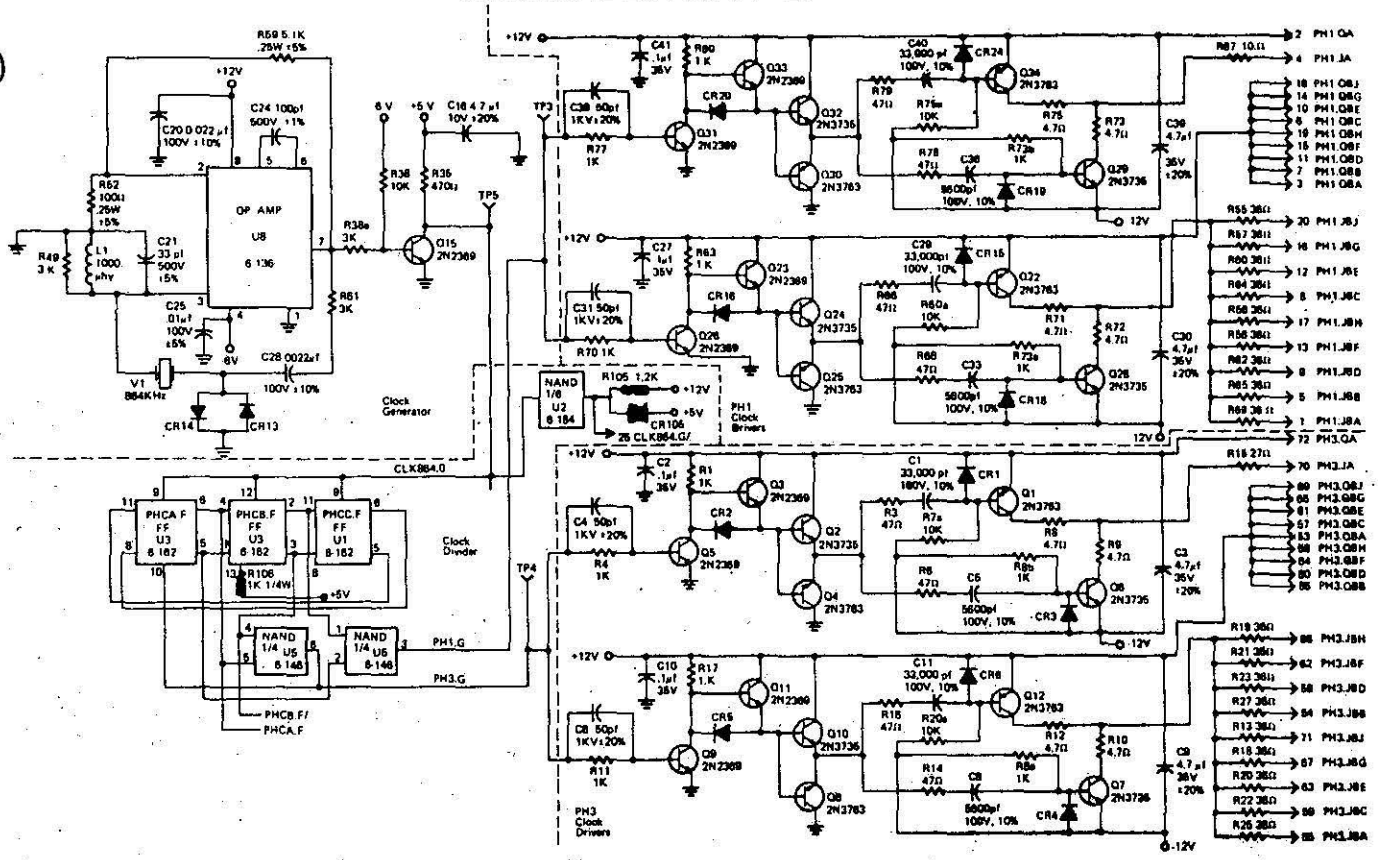
The M19-1 terminal clock module is provided with test points to aid the NCR Technical Services Representative in isolating system malfunctions caused by the M19-1. Table 1 shows the seven test points and the signal that can be monitored at each test point.

TEST POINT	FUNCTION
TP1	+12 v.d.c. monitor; this test point is at logic ONE when +12 v.d.c. power supply output is at least +11.04 v.d.c.
TP2	-12 v.d.c. monitor; this test point is at logic ONE when -12 v.d.c. power supply output is at least -11.04 v.d.c.
TP3	Phase 1 clock; signal at the test point goes from +5 v.d.c. to 0 v.d.c. for 1.157 μsec. every 6.94 μsec.
TP4	Phase 3 clock; signal at this test point goes from +5 v.d.c. to 0 v.d.c. for 1.157 μsec. every 6.94 μsec. PH3 is approximately 3.5 μsec. after PH1.
TP5	864-kHz clock; signal at this test point is a square wave having a 1.157 μsec. cycle time. The signal varies between +5 v.d.c. and 0 v.d.c.
TP6	Clock monitor; this test point is at logic ONE when the 864-kHz clock generator circuit is operable.
TP7	Logic ground

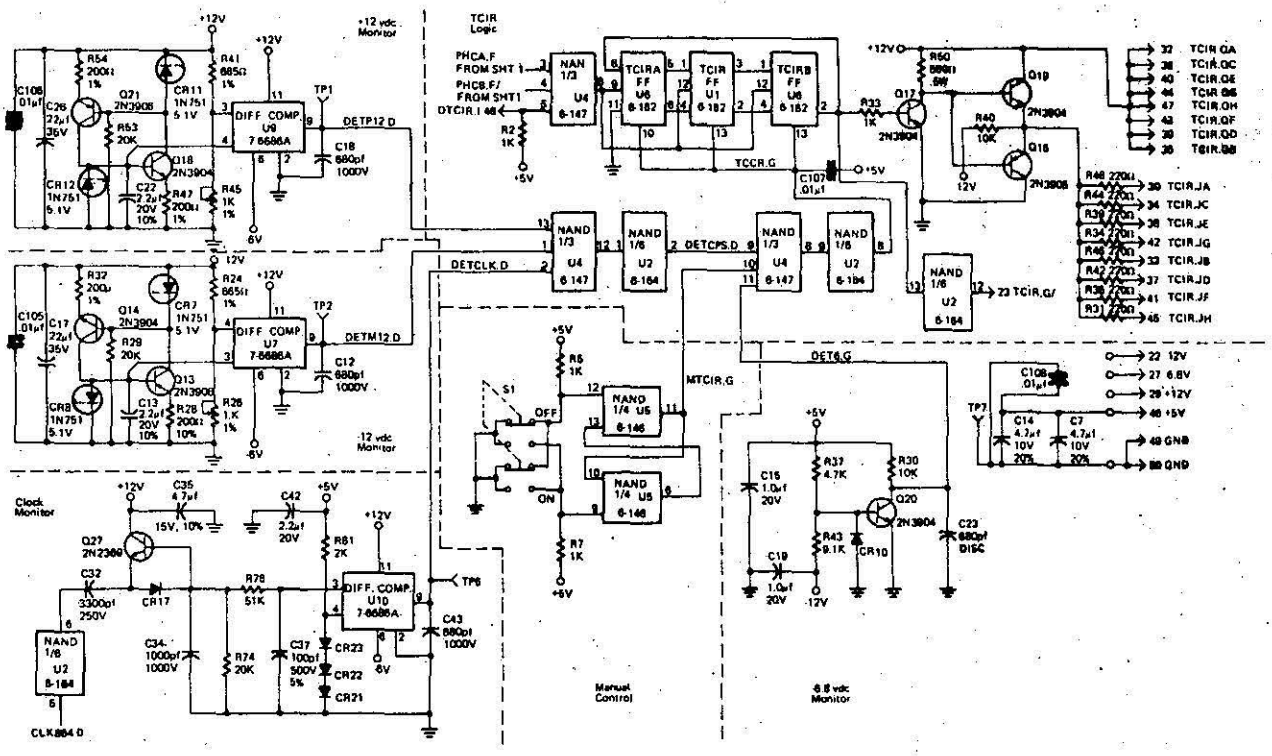
Table 1 M19-1 test points

Since the phase clock test points are connected in front of the clock drivers, the technician may have to check for the presence of the phase clocks at one of the module connectors. The technician should refer to the parent unit wire list to determine the appropriate pin to check.

TERMINAL CLOCK SCHEMATICS



TERMINAL CLOCK SCHEMATIC (SHEET 1)



TERMINAL CLOCK SCHEMATIC (SHEET 2)

Note: Shaded components found only on M19-1-280.